CLAIMS

What is claimed is:

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1. A processor comprising:
a replay queue to receive a plurality of instructions;
an execution unit to execute the plurality of instructions;
a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution, to increment a counter for each of the plurality of instructions to reflect the number of times each of the plurality of instructions has been executed, and to dispatch each instruction of the plurality of instructions to the execution unit either when the counter does not exceed a maximum number of replays or, if the counter for the instruction exceeds the maximum number of replays, when the instruction is safe to execute; and
a checker coupled to the execution unit to determine whether each instruction has executed successfully, and coupled to the replay queue to communicate to the replay queue each instruction that has not executed successfully.

2. The processor of claim 1 further comprising:
an allocator/renamer coupled to the replay queue to allocate and rename those of a plurality of resources needed by the instruction.

3. The processor of claim 2 further comprising:
a front end coupled to the allocator/renamer to provide the plurality of instructions to the allocator/renamer.

4. The processor of claim 2 further comprising:
a retire unit to retire the plurality of instructions, coupled to the checker to receive those of the plurality of instructions that have executed successfully, and coupled to the allocator/renamer to communicate a de-allocate signal to the allocator/renamer.

5. The processor of claim 4 wherein the retire unit is further coupled to the replay queue to communicate a retire signal when one of the plurality of instructions is retired.

6. The processor of claim 1 further comprising:
at least one cache system on a die of the processor;
a plurality of external memory devices; and
a memory request controller coupled to the execution unit to obtain data from the at least one cache system and the plurality of external memory devices.

7. The processor of claim 6 wherein the at least one cache system comprises a first level cache system and a second level cache system.

8. The processor of claim 6 wherein the external memory devices comprise at least one of a third level cache system, a main memory, and a disk memory.

9. The processor of claim 1 further comprising:
a staging queue coupled between the checker and the scheduler.

10. The processor of claim 1 wherein the scheduler comprises a plurality of counters to maintain each of the plurality of counters for each of the plurality of instructions.

11. The processor of claim 1 wherein the counter is one of a plurality of counters such that each counter of the plurality of counters is paired with one of the plurality of instructions.

12. The processor of claim 1 wherein the checker comprises a scoreboard to maintain a status of a plurality of resources.

13. A processor comprising:
a replay queue to receive a plurality of instructions;
at least two execution units to execute the plurality of instructions;
at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution, to increment a counter for each of the plurality of instructions to reflect the number of times each of the plurality of instructions has been executed, and to communicate each instruction of the plurality of instructions to the execution units when the counter does not exceed a maximum number or, if the counter for the instruction exceeds the maximum number of replays, when a data required by the instruction is available; and

a checker coupled to the execution units to determine whether each instruction has executed successfully, and coupled to the replay queue to communicate each instruction that has not executed successfully.

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14. The processor of claim 13 further comprising:

a plurality of memory devices coupled to the execution units such that the checker determines whether the instruction has executed successfully based on a plurality of information provided by the memory devices.

15. The processor of claim 13 further comprising:

an allocator/renamer coupled to the replay queue to allocate and rename those of a plurality of resources needed by the plurality of instructions.

16. The processor of claim 15 further comprising:

a front end coupled to the allocator/renamer to provide the plurality of instructions to the allocator/renamer.

17. The processor of claim 15 further comprising:

a retire unit to retire the plurality of instructions, coupled to the checker to receive those of the plurality of instructions that have executed successfully, and coupled to the allocator/renamer to communicate a de-allocate signal to the allocator/renamer.

18. The processor of claim 17 wherein the retire unit is further coupled to the replay queue to communicate a retire signal when one of the plurality of instructions is retired.

19. A method comprising:

receiving an instruction of a plurality of instructions;

placing the instruction in a queue with other instructions of the plurality of instructions;

speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies;

dispatching one of the plurality of instructions to an execution unit to be executed either when a counter for the instruction does not exceed a maximum number of replays or if the counter for the instruction exceeds the maximum number of replays, when a required data for the instruction is available;

executing the instruction;

determining whether the instruction executed successfully;

routing the instruction back to the queue if the instruction did not execute successfully; and

retiring the instruction if the instruction executed successfully.

20. The method of Claim 19 further comprising:

allocating those of a plurality of system resources needed by the instruction.

21. The method of Claim 20 wherein retiring comprises:

de-allocating those of the plurality of system resources used by the instruction being retired;

removing the instruction and a plurality of related data from the queue.

22. The method of Claim 19 further comprising:

maintaining a plurality of counters, one each for each of the plurality of instructions in the scheduler such that the counters reflect the number of times the corresponding instruction has been executed.

23. The method of Claim 22 wherein each of the plurality of counters for the instruction is paired with each of the plurality of the instructions.

24. The method of Claim 22 wherein the plurality of counters is stored in the scheduler.